Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A chip comprising:

a silicon ~~semiconductor~~ substrate;

a MOS device on a surface of said silicon substrate;

a metallization structure over said silicon ~~semiconductor~~ substrate, wherein said metallization structure comprises a first patterned circuit layer and a second patterned circuit layer over said first patterned circuit layer;

a dielectric layer between said first and second patterned circuit layers;

a passivation layer over said metallization structure, over said first and second patterned circuit layers and over said dielectric layer, wherein an opening in said passivation layer exposes a top surface of said metallization structure, wherein said passivation layer comprises a nitride layer and an oxide layer; and

a third patterned circuit layer comprising a first portion connected to said top surface through said opening and used to have a metal bump formed thereover, a second portion used to be in contact with a testing probe, and a third portion used to be wirebonded thereto, wherein said first portion is connected to said second portion.

Claim 2 (canceled)

3. (previously presented) The chip of Claim 1, wherein said second portion comprises a gold layer having a thickness of greater than 1 micron.

Claim 4 (canceled)

5. (currently amended) The chip of Claim 1, wherein said third patterned circuit layer comprises a gold layer and a nickel layer under said gold layer.

6. (currently amended) The chip of Claim 1, wherein said third patterned circuit layer comprises a gold layer and a copper layer under said gold layer.

7. (currently amended) The chip of Claim 1, wherein said third patterned circuit layer ~~further~~ comprises a copper layer, a nickel layer over said copper layer, and a gold layer over said nickel layer.

8. (currently amended) The chip of Claim 1 further comprising a polymer layer between said passivation layer and said third patterned circuit layer.

9. (previously presented) The chip of Claim 8, wherein said polymer layer comprises polyimide.

10. (currently amended) The chip of Claim 1 further comprising a polymer layer on said patterned circuit layer, multiple openings in said polymer layer exposing said first, second and third ~~second~~ portions.

11. (previously presented) The chip of Claim 10, wherein said polymer layer comprises polyimide.

Claim 12 (canceled)

13. (currently amended) The chip of Claim 1, wherein said third patterned circuit layer comprises ~~comprising~~ a metal trace connecting said first and second portions.

Claims 14 and 15 (canceled)

16. (currently amended) The chip of Claim 1, wherein said passivation layer has a thickness ~~of~~ greater than 0.35 μm.

17. (currently amended) The chip of Claim 1 further comprising ~~a~~ said metal bump over said first portion.

18. (currently amended) The chip of Claim 17 further comprising a nickel layer between said metal bump and said first portion.

19. (currently amended) The chip of Claim 17, wherein said metal bump comprises solder.

20. (currently amended) The chip of Claim 17 further comprising a copper layer between said metal bump and said first portion.

21. (currently amended) The chip of Claim 17, wherein said metal bump comprises a lead-free solder. ~~alloy.~~

Claims 22 and 23 (canceled)

24. (currently amended) The chip of Claim 1, wherein said third patterned circuit layer comprises a metal trace connecting said second and third portions.

25. (previously presented) The chip of Claim 1, wherein a pitch between said first and second portions is less than 300 μm.

26. (previously presented) The chip of Claim 1, wherein a pitch between said first and second portions is less than 1 millimeter.

27. (currently amended) A chip comprising:
a silicon ~~semiconductor~~ substrate;
a MOS device on a surface of said silicon substrate;
a metallization structure over said silicon ~~semiconductor~~ substrate, wherein said

metallization structure comprises a first patterned circuit layer and a second patterned circuit layer over said first patterned circuit layer;

a dielectric layer between said first and second patterned circuit layers;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure, and wherein said passivation layer comprises a nitride layer and an oxide layer; and

a third patterned circuit layer comprising a metal trace over said passivation layer and connected to said top surface through said opening, a first portion used to have a metal bump formed thereover and connected to said metal trace, and a second portion comprising a copper layer and a nickel layer over said copper layer of said second portion, wherein said copper and nickel layers of said second portion are used to be wirebonded thereover.

28. (previously presented) The chip of Claim 27, wherein said second portion further comprises a titanium-containing layer under said copper layer.

29. (previously presented) The chip of Claim 27, wherein said second portion further comprises a chromium-containing layer under said copper layer.

30. (currently amended) The chip of Claim 27 further comprising a polymer layer between said passivation layer and said third patterned circuit layer.

31. (previously presented) The chip of Claim 30, wherein said polymer layer comprises polyimide.

32. (currently amended) The chip of Claim 27 further comprising a polymer layer on said third patterned circuit layer, multiple openings in said polymer layer exposing said first and second portions.

33. (previously presented) The chip of Claim 32, wherein said polymer layer

comprises polyimide.

34. (previously presented) The chip of Claim 27, wherein said metal trace connects said first and second portions.

35. (currently amended) The chip of Claim 27, wherein said third patterned circuit layer comprises a third portion used to be in contact with a testing probe.

Claim 36 (canceled)

37. (previously presented) The chip of Claim 35, wherein said metal trace connects said first and third portions.

38. (previously presented) The chip of Claim 27, wherein said passivation layer has a thickness ~~of~~ greater than 0.35 μm.

Claim 39 (canceled)

40. (currently amended) The chip of Claim 27 further comprising ~~a~~ said metal bump over said first portion.

41. (currently amended) The chip of Claim 40, wherein said metal bump comprises solder.

42. (currently amended) The chip of Claim 40 further comprising an under-bump-metallurgy (UBM) ~~a nickel~~ layer between said metal bump and said first portion, wherein said under-bump-metallurgy (UBM) layer comprises nickel.

43. (currently amended) The chip of Claim 40, wherein said metal bump comprises a lead-free solder, ~~alloy.~~

44. (previously presented) The chip of Claim 27 further comprising a wirebonded wire bonded over said second portion.

Claims 45-51 (canceled)

52. (currently amended) The chip of Claim 27, wherein said second portion further comprises a gold layer over said nickel ~~copper~~ layer.

53. (previously presented) The chip of Claim 27, wherein said metal trace comprises a copper layer.

54. (previously presented) The chip of Claim 53, wherein said metal trace further comprises a nickel layer over said copper layer of said metal trace.

55. (previously presented) The chip of Claim 54, wherein said metal trace further comprises a gold layer over said nickel layer of said metal trace.

56. (previously presented) The chip of Claim 27, wherein said first portion comprises a copper layer.

57. (previously presented) The chip of Claim 56, wherein said first portion further comprises a nickel layer over said copper layer of said first portion.

58. (previously presented) The chip of Claim 57, wherein said first portion ~~metal trace~~ further comprises a gold layer over said nickel layer of said first portion.

59. (previously presented) The chip of Claim 1, wherein said second portion comprises a gold layer.